

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Production

Revision 1.1: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52250STDR	Tape & Reel	4000	2250	8	SOP-8L

Over ope

$V_{IN}=12V$, $T_A=25^{\circ}C$.

Figure 1. UVLO vs Temperature

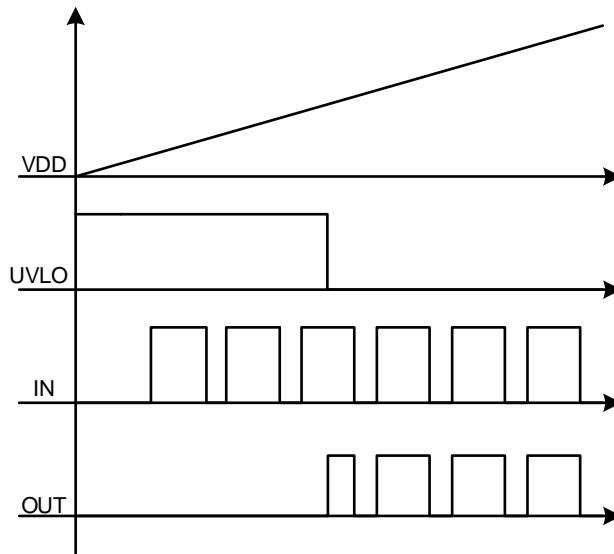
Figure 2. Supply current vs Temperature

Figure 3.

SCT52250

Overview

The SCT52250 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 5A peak current along with the minimum propagation delay 12ns from input to output. The 1ns delay matching and the stackable output characteristics



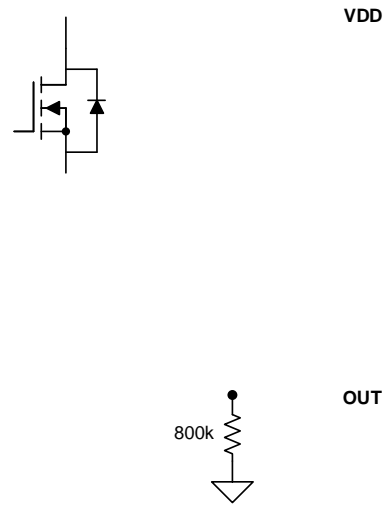


Figure 12

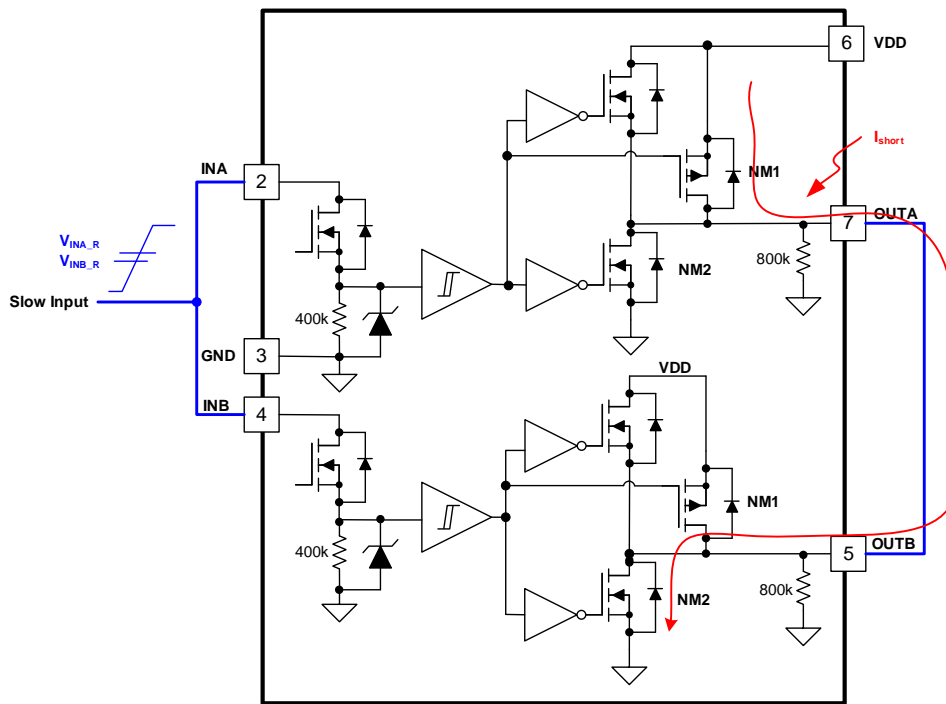


Figure 13. SCT52250 Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

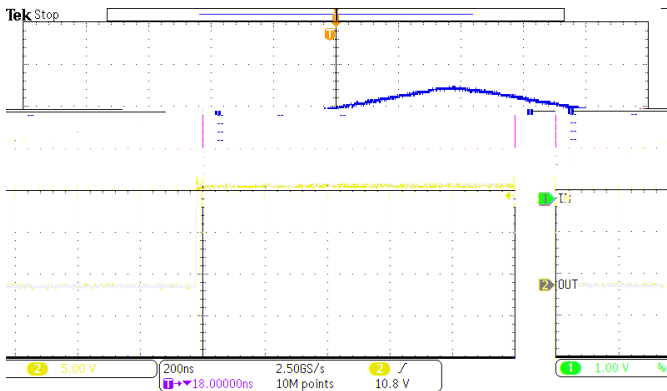


Figure 14. Driver Switching ON

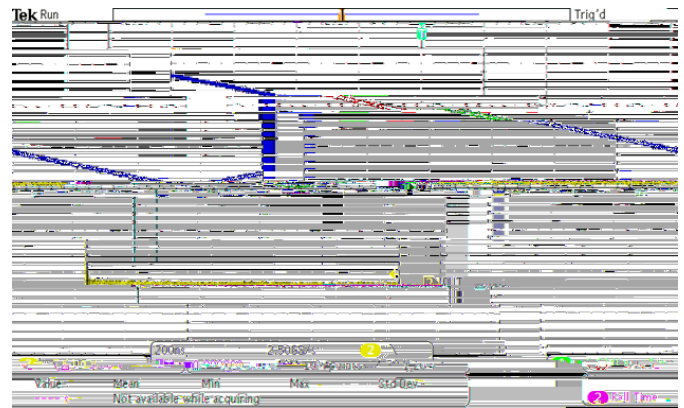


Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52250 exceeds 162 C, the thermal sensing circuit stops switching until the junction temperature falling below 137 C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Typical Application

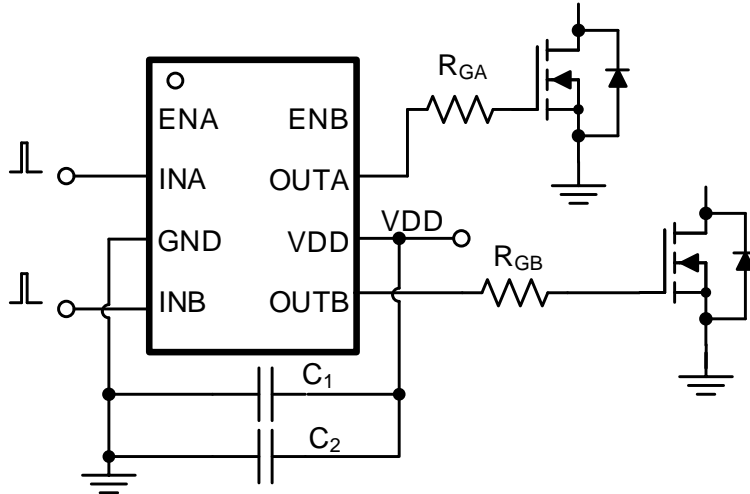


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52250 depends on the gate charge required of the power device (Q_g), switching frequency, and use of external gate resistors. The SCT52250 features very low quiescent current and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52250 is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52250 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT52250
- R_{OL} is the pull down resistance of SCT52250
- R_G is the gate resistance between driver output and gate of power device.

Application Waveforms

VDD=12V unless otherwise noted

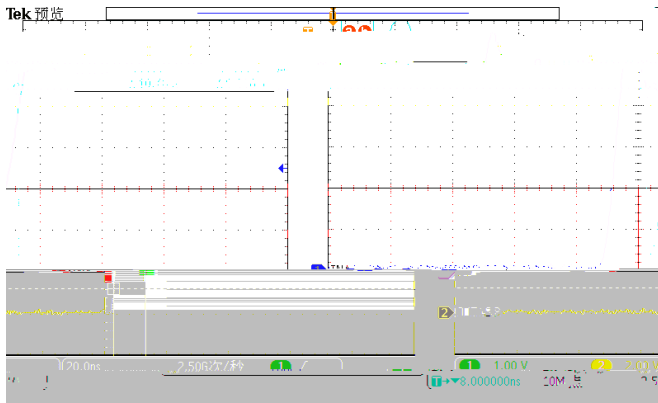


Figure 23. Stackable Output Rise (Out capacitance=3.3nF)

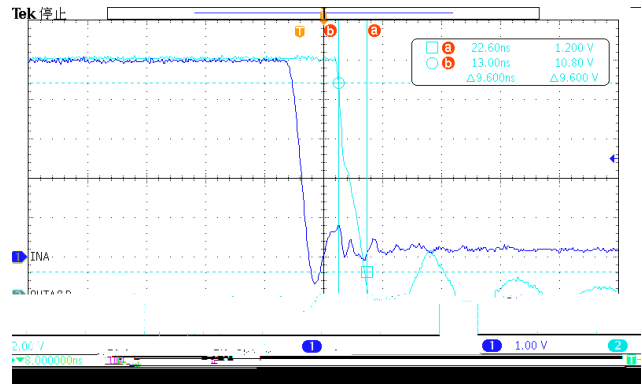


Figure 24. Stackable Output Fail (Out capacitance=3.3nF)

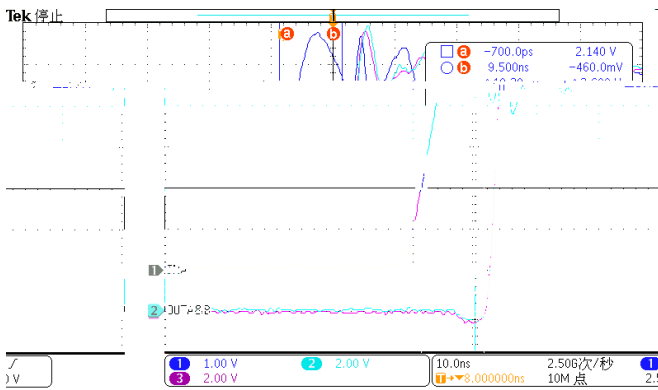


Figure 25. Delay Matching Rise (Out capacitance=1.8nF)

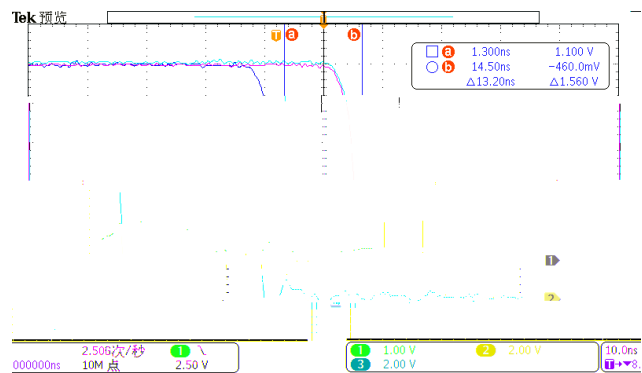


Figure 26. Delay Matching Fail (Out capacitance=1.8nF)

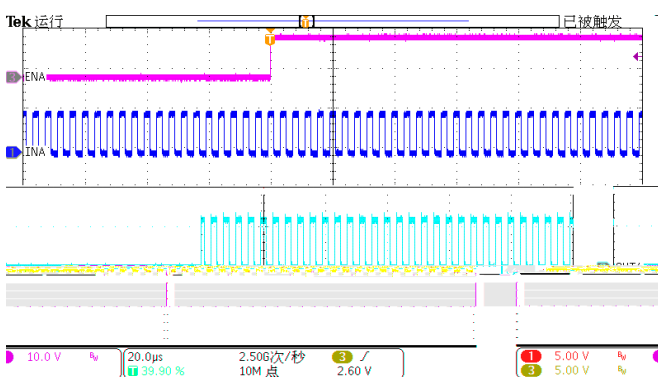


Figure 27. Enable

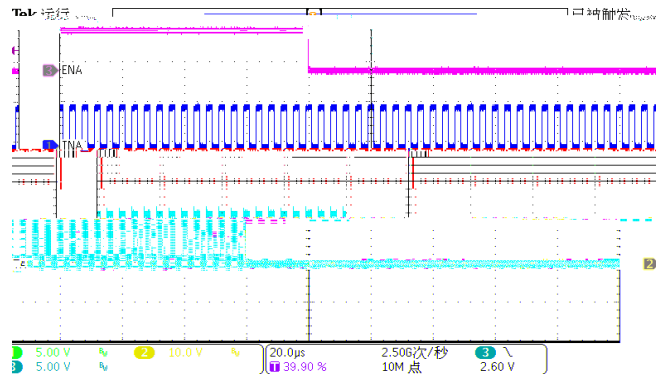


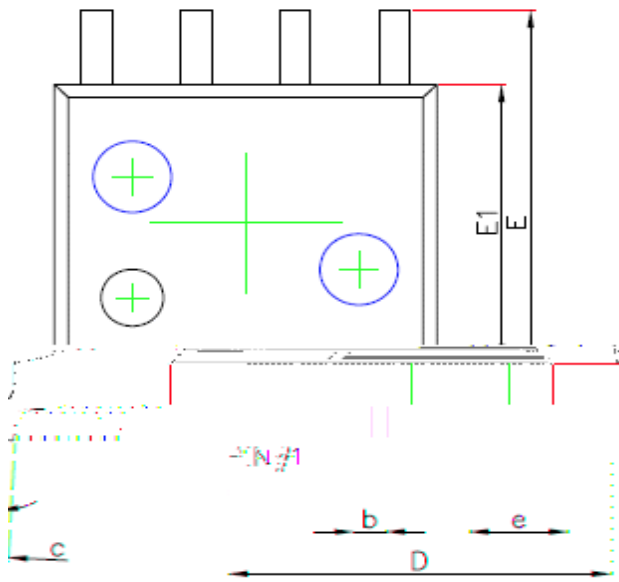
Figure 28. Disable

SCT52250

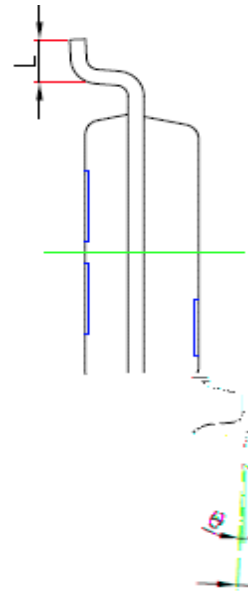
Layout Guideline

The SCT52250 provides the 5A output driving current and features very short rise and fall times at the power device gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI problems if the power device gate driver has too much parasitic inductance.

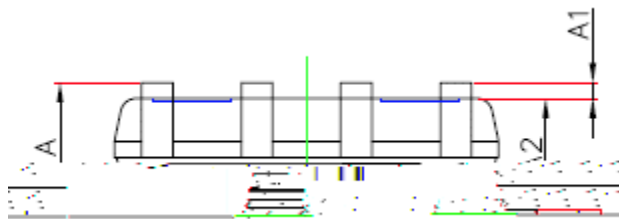
Put the SCT52250 as close as possible to the power device to minimize the gate driving loop inductance. Decoupling the driver output and power device gate with a decoupling capacitor.



TOP VIEW



BOTTOM VIEW

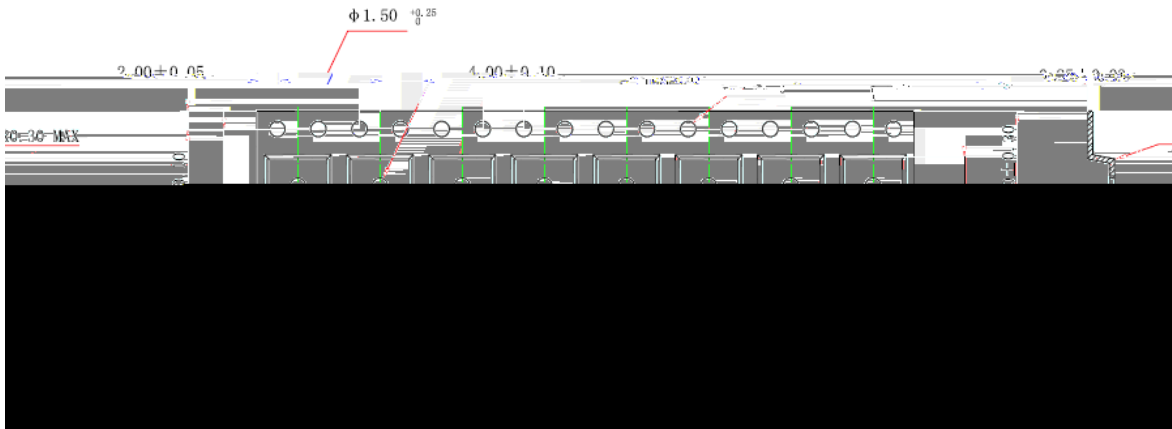
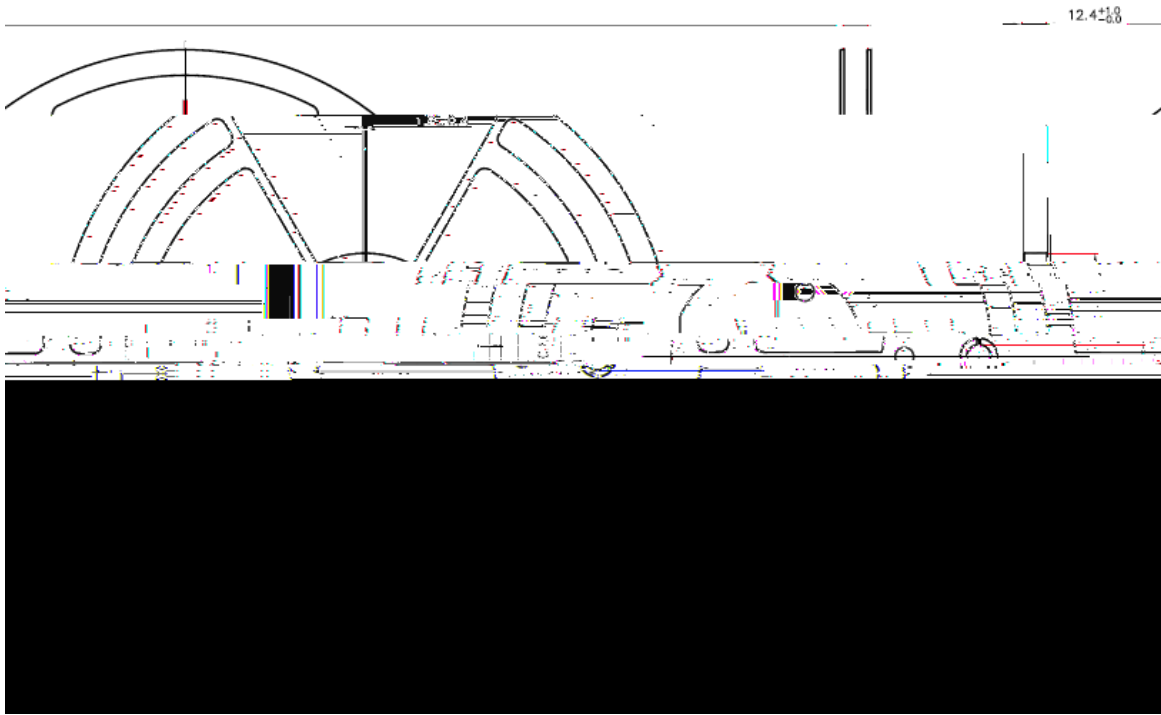


SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°



Feeding Direction

