REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

Revision 1.1: Update the Figure 8 and Figure 26 and thermal performance on page 20.

Revision 1.2: Add MSL level in device order information. Update tape and reel information.

DEVICE ORDER INFORMATION

SCT71010A00QDTBR	Adjust	DFN3x3-8	0A00Q	8	1	Tape & Reel, 5000

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Product Folder Links

ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT}+1V$, $C_{OUT}=10uF$, T_J= -40°C~125°C, typical value is tested under 25°C.

V_{EN_Hys}	Enable threshold hysteresis	$V_{EN_Hys_3.3}(V_{IN}=3.3V)$	85		mV
		$V_{EN_Hys_5}(V_{IN}=5V)$	180		
I_{EN_0V}	Enable pin current	EN=0		0.2	εA
$I_{EN_3.3V}$	Enable pin current	EN=3.3V	0.01	0.2	εA
$R_{EN_pulldown}$	enable pulldown resistor		648		kq
T_{SS}	Soft-start time		2.4		ms

V_{PG_R}	PG rising threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} rising	88%		
V_{PG_F}	PG falling threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} falling	82%		
V_{PG_LOW}	PG output low voltage	PG sink 0.5mA	84		mV

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TYPICAL CHARACTERISTICS (continued)

Figure

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TYPICAL CHARACTERISTICS (continued)

Figure 11. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,COUT=10uF

Figure 12. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,IOUT=10mA

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TYPICAL CHARACTERISTICS (continued)

Figure 13. PSRR vs Frequency
VIN=4.3V, Cf=33pF,COUT=10uF,IOUT=10mA

Figure 14. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,COUT=10uF

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FUNCTIONAL BLOCK DIAGRAM

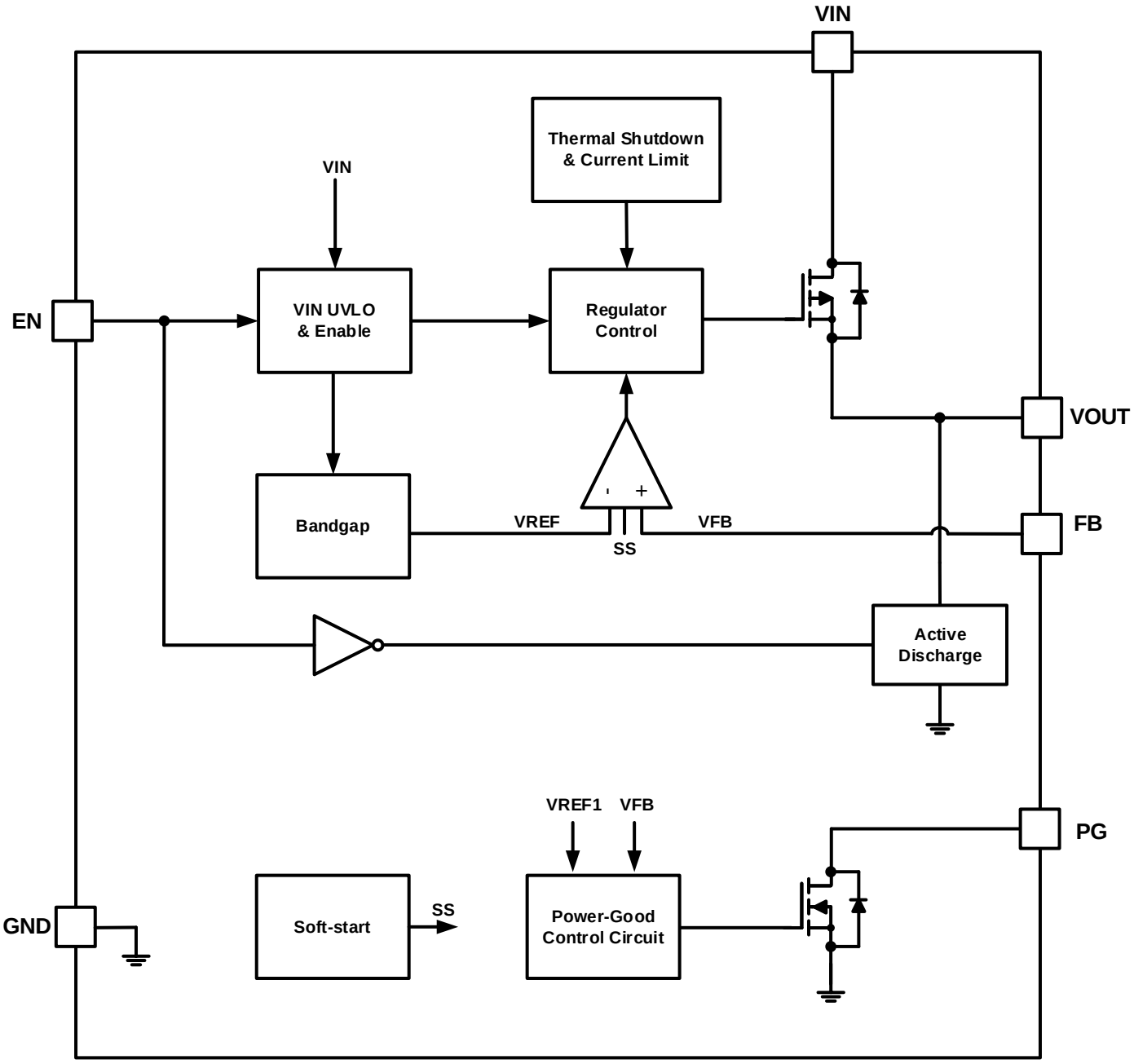

Figure 15. Functional Block Diagram of Adjust Output Version

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The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN}–V_{OUT})Ï I_{OC}]. When the output is shorted and the output voltage is less than $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN}–V_{OUT})Ï I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

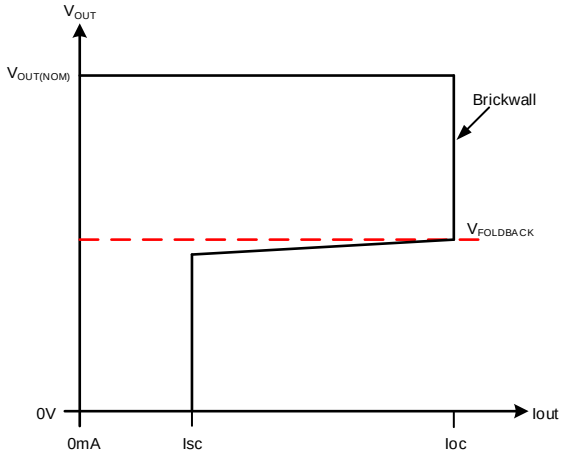

Figure 16. Current Limit with Foldback Feature

The SCT71010A00Q product integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 2.4ms. If the EN pin is pulled below 0.66V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limit by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by foldback current limit (I_{SC}) at VOUT<$V_{FOLDBACK}$, and the slope of VOUT is limited by over current limit (I_{OC}), when VOUT> $V_{FOLDBACK}$.

In SCT71010A00Q product, typical Tss is 2.4ms, and typical I_{OC} is 1450mA and typical Isc is 480mA, could use the following formula for initial startup time calculation.

(1)

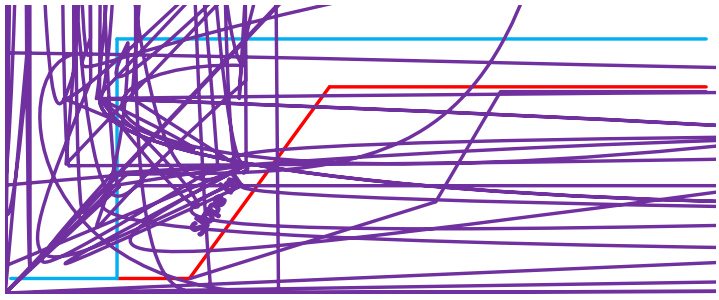

Figure 17. Soft-start Waveform vs Output Capacitor

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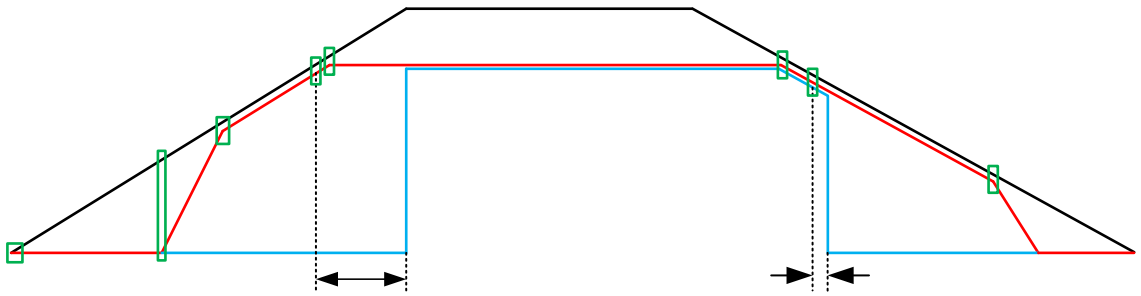

Figure 20. Startup and Shutdown Example —SCT71010Q Series

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

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backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220εF. Also by inserting a reverse polarity diode in to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

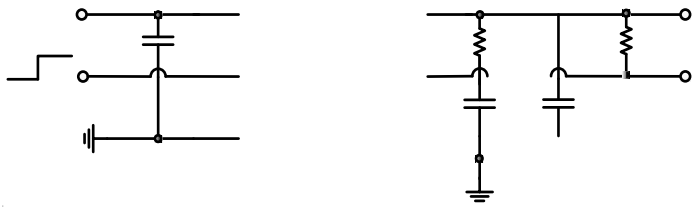

Figure 23. SCT71010A00Q Typical Application Schematic with Large Output Capacitor

Input Voltage	5V Normal, 2.2V~5.5V
Output Voltage	0.8V~5V
Maximum Output Current	1A
Output Capacitor Range (C_{OUT1} and ESR)	2.2uF~220uF with ESR=0.5q ~5q
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

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Figure 24. SCT71010A00Q Feed Forward Capacitors recommend(R2=100kq ,VOUT=1.8V)

Figure 25. SCT71010A00Q Feed Forward Capacitors recommend(R2=10kq ,VOUT=1.8V)

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Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3. Because $I_{GND} \ll I_{OUT}$, the term $V_{IN} \times I_{GND}$ in Equation 3 could be ignored.

(3)

The junction temperature can be estimated using Equation 4. $R_{\theta JA_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J.

(4)

$R_{\theta JA_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71010A00Q product, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the R_{JA_EVM} of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 4-layer,1oz Cu (inner 0.5oz Cu), 50mm x 30mm size.

DFN3X3-8	2.73	1.88	53.09

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THERMAL CHARACTERISTICS

Figure 26. Maximum Output Current vs Input Voltage, VOUT=1.8V of DFN3X3 ,$T_J \leq$ TSD_R

Figure 27. Maximum Output Current vs Input Voltage, DFN3X3,TJ ≤ 125

Figure 28. Maximum Allowed Power Dissipation vs Ambient Temperature, DFN3X3,TJ ≤ 125

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Vin=Vout +1V, unless otherwise noted

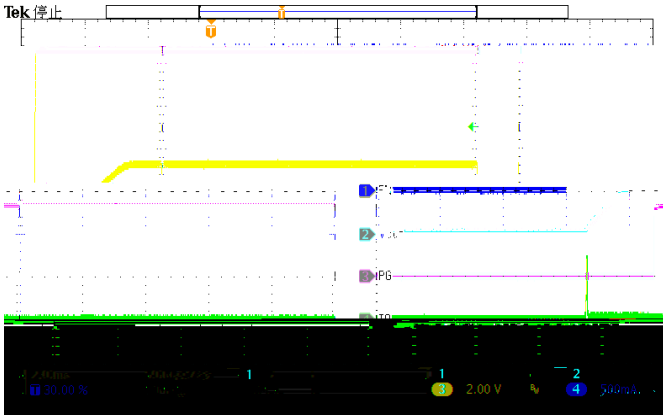

Figure 35. Enable (Iload=10mA)

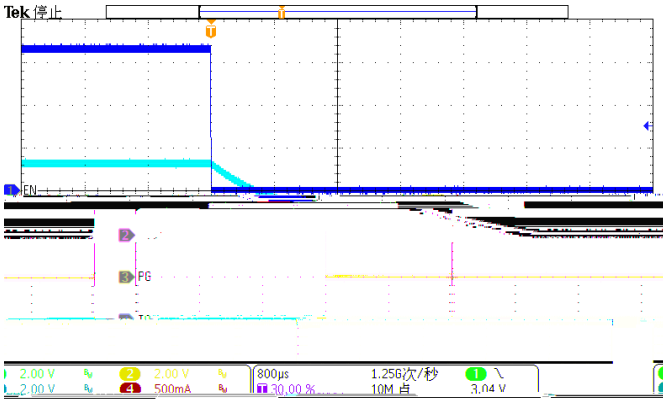

Figure 36. Disable (Iload=10mA)

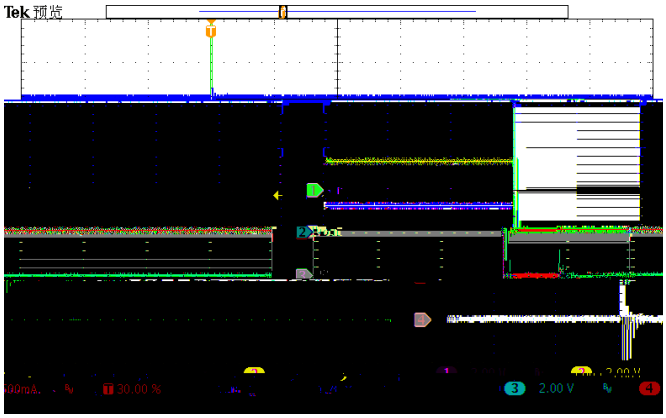

Figure 37. Enter Short Circuit Protection

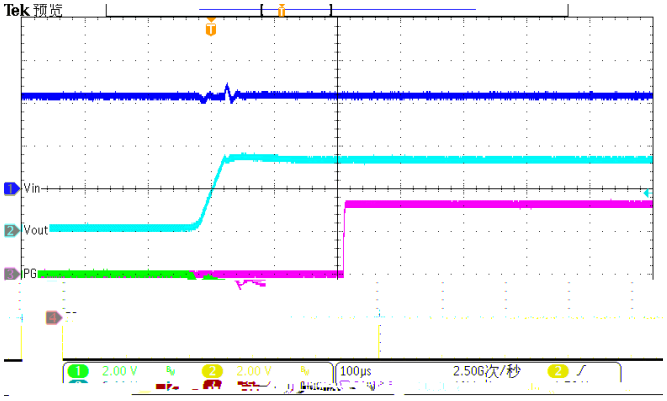

Figure 38. Exit Short Circuit Protection

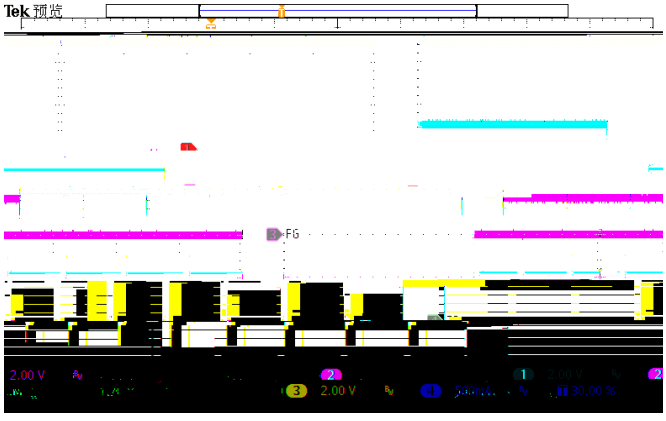

Figure 39. Enter Over Temperature Protection(Vin=5.5V)

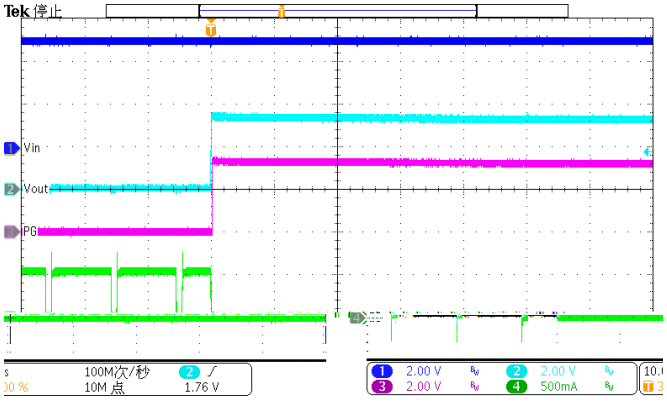

Figure 40. Exit Over Temperature Protection(Vin=5.5V)

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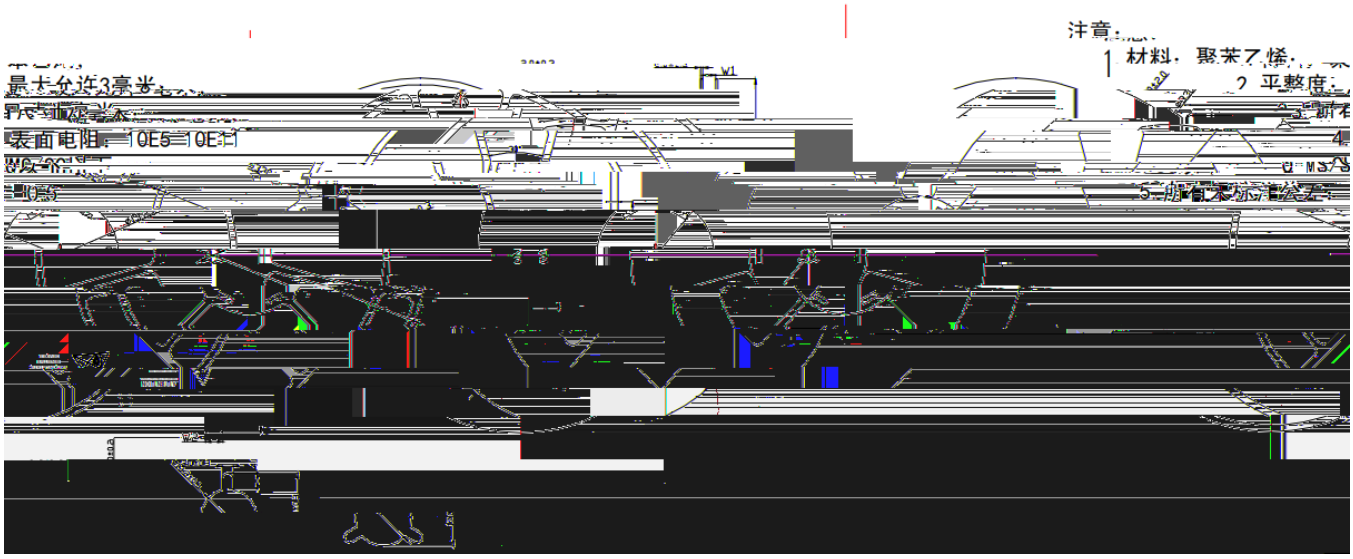
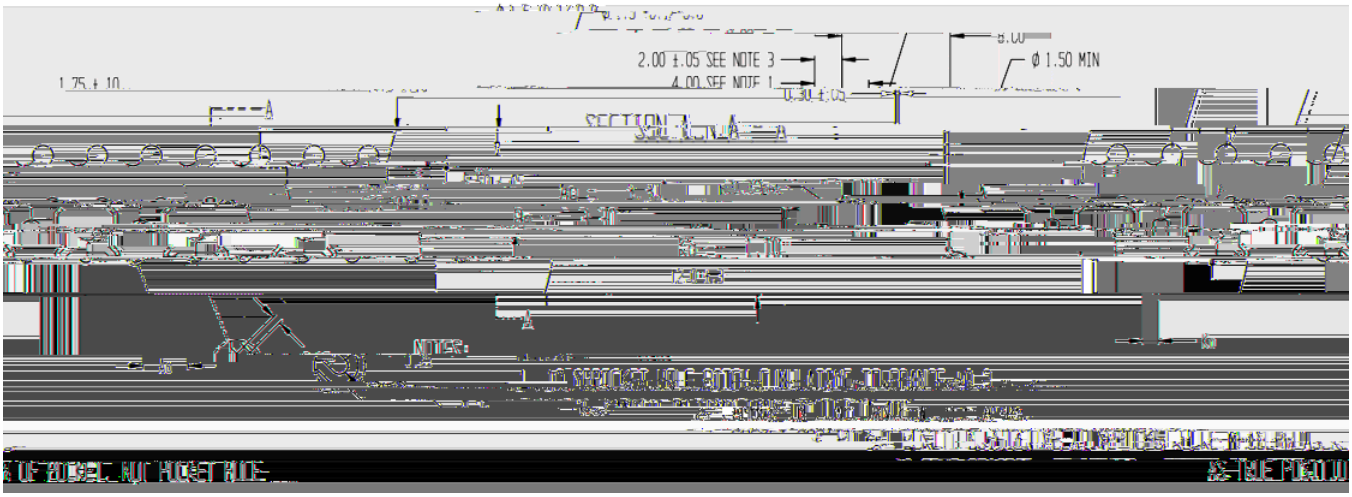
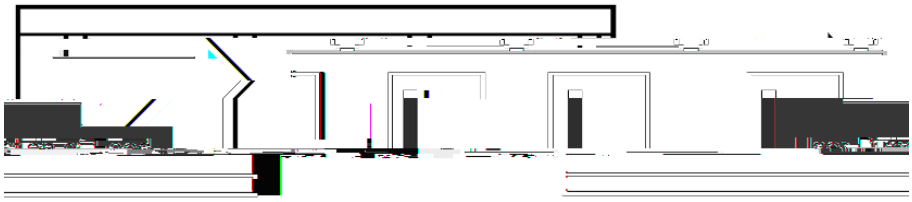
TAPE AND REEL INFORMATION







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