3.6V-36V Vin, 3A, High Efficiency Synchronous Step-down DCDC Converter

AEC-Q100 Qualified with the Following Results:
- Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Device HBM ESD Classification Level H2
- Device CDM ESD Classification Level C3B

Wide Input Range: 3.6V-36V

Up to 3A Continuous Output Current

0.8V Feedback Reference Voltage

Integrated 60mΩ High-Side and 36mΩ Low-Side Power MOSFETs

Pulse Skipping Mode (PSM) with 30uA Quiescent Current in Sleep Mode

60ns Minimum On-time

4ms Internal Soft-start Time

Adjustable Switching Frequency: 200k~2.2MHz

Frequency Spread Spectrum (FSS) Modulation for EMI Reduction

Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis

Parallel input path to minimize switch node ringing

Low Dropout Mode Operation

Over-voltage and Over-Temperature Protection

Available in 2mm*3mm QFN-12L Package

Automotive infotainment and ADAS

USB Type-C Power Delivery, USB Charging

Industrial and Medical Distributed Power Supplies

The SCT2434DQ is 3A synchronous buck converters with wide input voltage, ranging from 3.6V to 36V, which integrates a 60mΩ high-side MOSFET and a 36mΩ low-side MOSFET. The SCT2434DQ, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 30uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2434DQ features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency can be set between 200kHz and 2.1MHz through a resistor. The SCT2434DQ allows power conversion from high input voltage to low output voltage with a minimum 60ns on-time of high-side MOSFET.

The SCT2434DQ is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2434DQ features Frequency Spread Spectrum FSS with ±10% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conduct e SM b

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Released to Market

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2434DQFPAR	Tape & Reel	5000	434DQ	12	FCQFN2x3-12L	1

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	42	V
EN	-0.3	42	V
BOOT	-0.3	48	V
SW	-1	42	V
BOOT-SW	-0.3	6	V
PG	-0.3	24	V
FB	-0.3	6	V
Operating junction temperature TJ(3)	-40	150	°C
Storage temperature TSTG	-65	150	°C

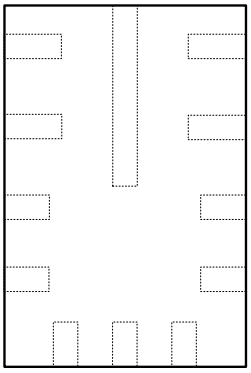

Figure 1. 12-Lead QFN 2mm×3mm

PG	8	Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PG output goes low when EN =low, VIN > 1V.

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.6		36	V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

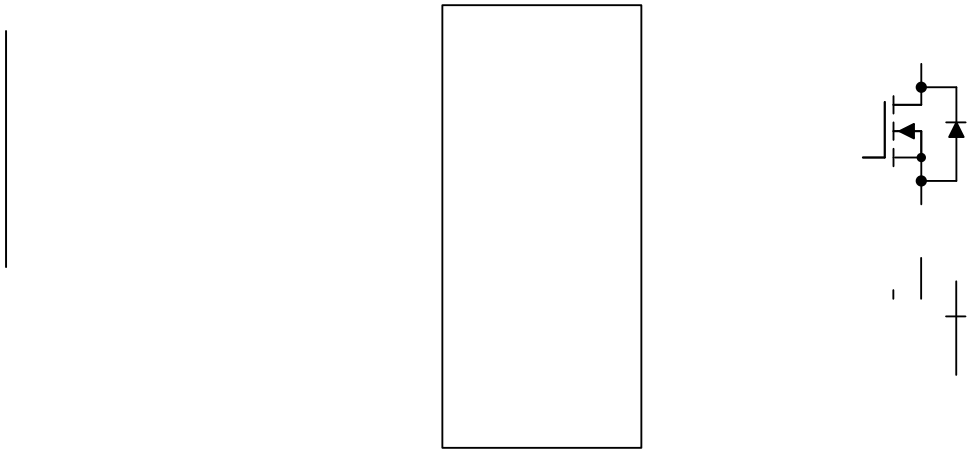

Figure 8. Functional Block Diagram

Overview

The SCT2434DQ is a 3.6V-36V input, 3A output, EMI friendly synchronous buck converter with built-in 60mΩ Rdson high-side and 36mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 1.8MHz. The SCT2434DQ features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 30uA under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2434DQ implements the Frequency Spread Spectrum FSS modulation spreading of ±10% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2434DQ full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2434DQ employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output volta

Enable and Under Voltage Lockout Threshold

The SCT2434DQ is enabled when the VIN pin voltage rises about 3.4V and the EN pin voltage exceeds the enable threshold of 1.24V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.12V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

(1)

Fsw	R_6 (R_{FSW})
200 KHz	182 KΩ
300 KHz	120 KΩ
355 KHz	

Figure 10. LDO Operation Characteristic (V_{OUT}=5V)

Over Current Limit and Hiccup Mode

are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 130us deglitching time do not trip the PG flag.

Thermal Shutdown

The SCT2434DQ protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 160°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 140°C, the device restarts with internal soft start phase.

Output Voltage

The output voltage is set by an external resistor divider R_3 and R_4 in typical application schematic. When the output voltage is greater than 3V, recommended R_4 resistance is 24.9KΩ. Use Equation 4 to calculate R_3.

(4)

where:

V_{REF} is the feedback reference voltage, typical 0.8V

(6)

where:

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

I_1=1uA, I_2=3.8uA, V_{ENR}=1.24V, V_{ENF}=1.12V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and

I_{LPP} is the inductor peak-to-peak current
I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2434DQ can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.3 to 0.5, and the inductor value is calculated to be 1.7uH, the RMS inductor current is 3A and the peak inductor current is 3.6A. The chosen inductor is a WE 74439358022, which has a saturation current rating of 12.55A. This also has a typical inductance of 2.2µH at no load and 2.19 µH at 3A load. The inductor DCR is 3.7mΩ.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

Application Waveforms

V_{IN}=12V, V_{OUT}=5V, unless otherwise noted

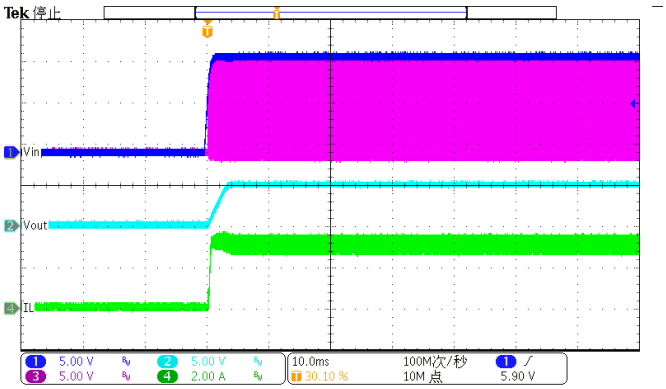

Figure 12. Power up(I_{LOAD}=3A)

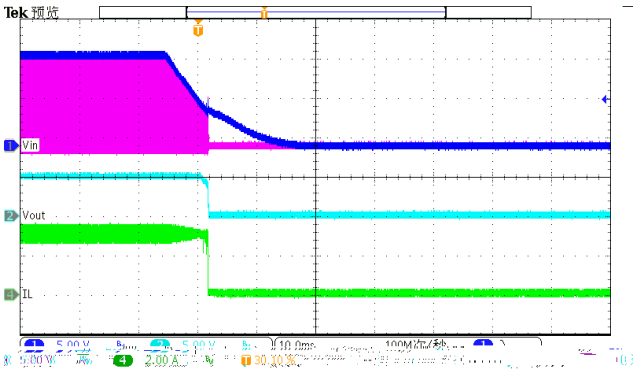

Figure 13. Power down(I_{LOAD}=3A)

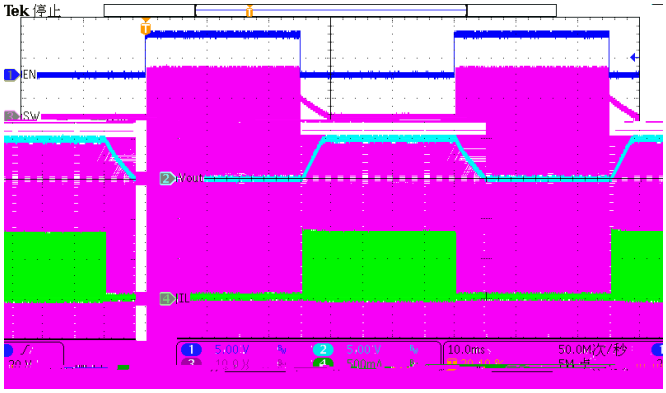

Figure 14. EN toggle (I_{LOAD}=0.1A)

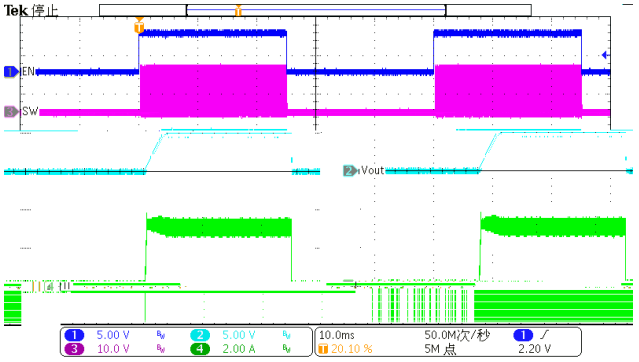

Figure 15. EN toggle (I_{LOAD}=3A)

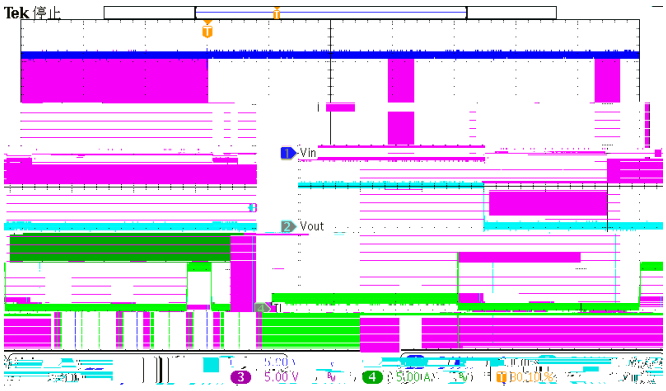

Figure 16. Over Current Protection(1A to hard short)

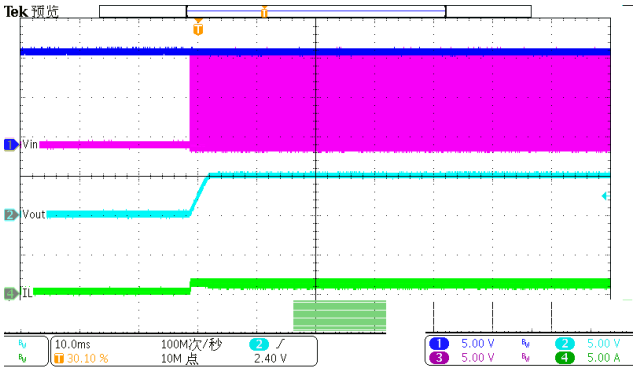

Figure 17. Over Current Release (hard short to 1A)

Application Waveforms

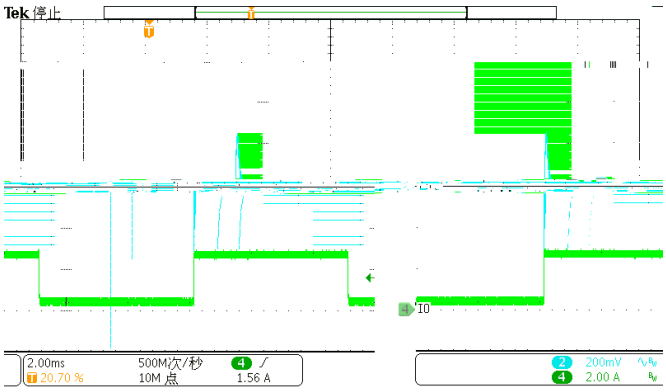

Figure 18. Load Transient (0.3A-2.7A, 1.6A/us)

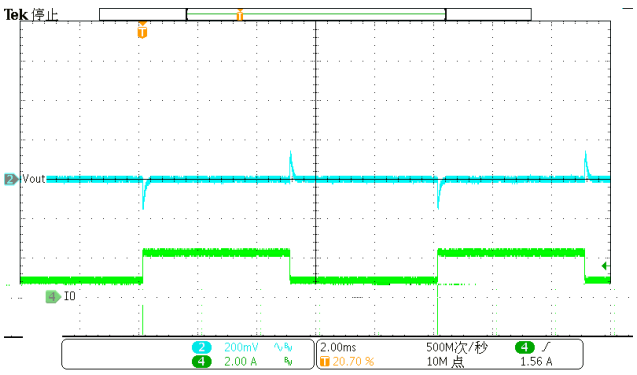

Figure 19. Load Transient (0.75A-2.25A, 1.6A/us)

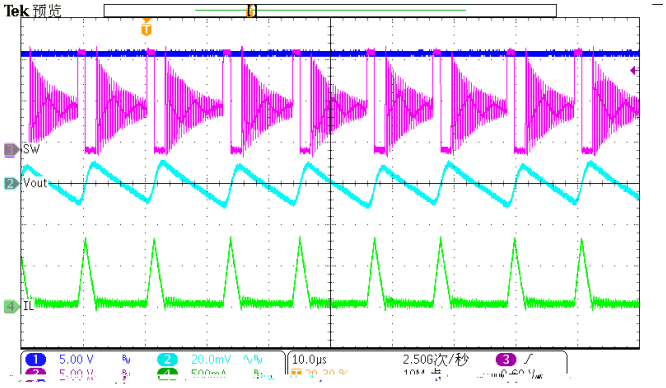

Figure 20. Output Ripple (I_{LOAD}=100mA)

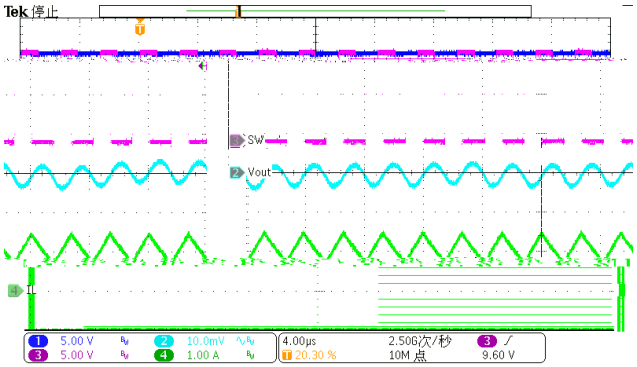

Figure 21. Output Ripple (I_{LOAD}=1A)

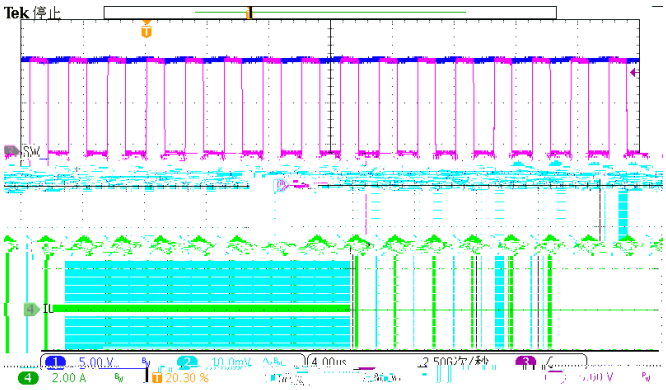

Figure 22. Output Ripple (I_{LOAD}=3A)

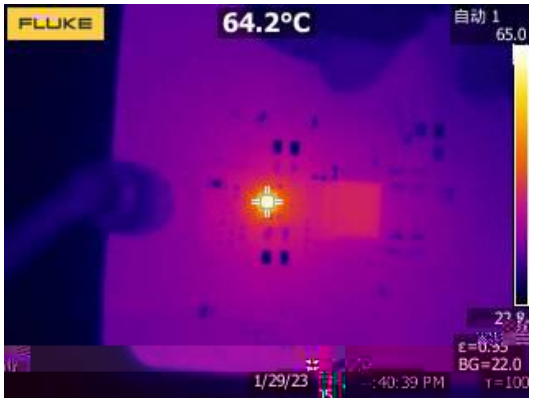

Figure 23. Thermal, $12V_{IN}$, $5V_{OUT}$, 3A

Layout Guideline

Proper PCB layout is a critical for SCT2434DQ's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and PGND as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. UVLO adjust and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
5.